**Experiment 10 – Full Adder**

**Objective:**

Write the code to design a BCD to Binary convertor and write its test bench is System Verilog.

**Tool Used:**

Xilinx ISE.

**Theory:**

$urandom\_range sets the random value between the range 0 to the value specified inside the brackets.

**Code:**

**DUT:**

module bcd(input [7:0]x, output reg [7:0] y);

  assign y = x[7:4]\*10 + x[3:0];

endmodule

**TB:**

module bcdtb();

  reg [7:0]x;

  wire [7:0] y;

  bcd dut(x,y);

  initial begin

    $monitor("@time:%3d,for input = %h output = %h",$time, x, y);

    repeat(10)begin

      x[7:4] = $urandom\_range(9);

      x[3:0] = $urandom\_range(9);

      #1;

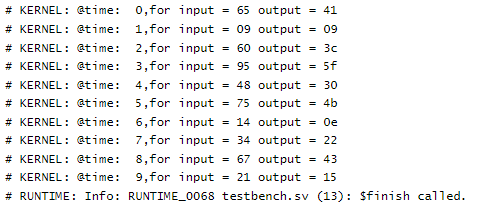
    end

    $finish;

  end

endmodule

**Output:**

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**Result:**

The given problem statement is executed and verified to be correct.